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EXAMINER	
CHANG, EDITH M	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/618,645	GRIFFIN, GRANT R.	
	Examiner	Art Unit	
	Edith M. Chang	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,14-24 and 28-38, 40-44* is/are rejected.

7)☒ Claim(s) *11-13,25-27 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on November 12, 2004. These drawings are acceptable.

Response to Arguments/Remarks

2. Applicant's arguments filed on November 12, 2004 have been fully considered but they are not persuasive. The rejections of claims 1-10, 14-24, 28-42 are upheld, the rejections of clams 11-13, 25-27 and 39 are withdrawn.

Argument: Applicant argues that the pilot up and down chirps contained in the received signal are different from a reference training sequence Citta reference.

Response: In Citta reference, column 2 lines 21-31 teaches the pilot chirps contained in the received signal correlated with a reference chirps to synchronize the receiver, wherein the pilot chirps synchronize the demodulator with the timing error, hence the reference chirps/samples furnish the training sequences according to the definition of the training sequence described on page 1 lines 14-17 and page 2 lines 7-9 of the current application; and in Figure 6 shows the first 100 samples (a sequence) of the reference chirps, the x axis is labeled by the sample index numbers 1 to 100. Therefore, Citta teaches the training sequence.

Argument: "low-level noise transmission does not constitute a reference training sequence as provided in Applicant's claims".

Response: In Applicant's claims provide merely "a reference training sequence".

Argument: Citta does not teach or suggest determining if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization and calculate a required fractional sample delay to improve synchronization.

Response: In Figure 7 the synchronizer 46 with the feedback from the FPLL 62 (frequency/phase lock loop, column 6 lines 40-44) to determine the improvement (locked or not) and from the Timing block 64 to calculate the timing error (Figure 9-12) for Delay block 68. The delay imposed by the timing block 64 has an integer part and a fraction part (shown in Figure 14, column 11 lines 60-61), wherein the integer part is for a multiplexer (column 11 lines 64-67) the fractional part is used to determine a fractional of a sample to be advanced or retarded (column 11 line 67-column 12 line 4). Therefore, Citta teaches and suggests the limitation as cited in the claims.

Claim Objections

3. Claims 1-40 and 43-44 are objected to because of the following informalities:

Claim 1, lines 4 & 13: "the digital data" is suggested changing to "the transmitted digital Data; line 11: "a fractional" is suggested changing to "the fractional".

Claims 2 & 16 line 2 & Claims 3 & 17 line 3: "a fractional" is suggested changing to "the fractional".

Claims 4-5 & 18-19, line 3: "a threshold" is suggested changing to "the threshold".

Claim 11, line 4: "adder/summer" is suggested changing to "adder or summer".

Claim 15, line 11: "a fractional" is suggested changing to "the fractional"; line 13: "the digital data" is suggested changing to "the received digital data".

Claims 20 & 21, line 2: "step further" is suggested changing to "step".

Claims 26 & 27, line 2: "a fractional" is suggested changing to "the fractional".

Claim 31, line 1: "computer executable code" should be "computer executable code stored in a computer readable medium" for executing.

Claims 6-10, 12-14, 22-23, 25, 28-30, 32-40 and 43-44 are directly or indirectly dependent on objected claims 1, 15 and 31.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 10, 15-16, 24, 29, and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Citta et al. (US 6304619 B1) in view of Krasner (US 6208291 B1).

Regarding **claims 1 & 15**, Citta et al. discloses a demodulator and its methods for demodulating digital data (Figure 5), comprising: *a receiver* for receiving a digital data signal (42-44 Figure 5 is the receiver); *a correlator* (158 Figure 10) to correlate the digital signal received from the receiver with a reference training sequence (column 2 lines 21-31, column 3 lines 29-31 wherein the reference chirps furnish a reference training sequence) to produce a correlation value; *a verification unit* (166 Figure 10) to select correlation values (Figure 8 is an example of correlation results/values); in Figure 7 the synchronizer 46 with the feedback from

the FPLL 62 (frequency/phase lock loop as *determine device*, column 6 lines 40-44) to determine the improvement (locked or not) and from the Timing block 64 to calculate the timing error (Figure 9-12) for Delay block 68. The delay imposed by the timing block 64 has an integer part and a fraction part (shown in Figure 14, column 11 lines 60-61), wherein the integer part is for a multiplexer (column 11 lines 64-67) the fractional part is used to determine a fractional of a sample to be advanced or retarded (column 11 line 67-column 12 line 4); *an implementing device* (Figure 14 Fraction) implementing the fractional sample delay if said determining device determines that a fractional sample delay would improve the demodulation synchronization timing; and a demodulating device for demodulating the digital data signal (50 Figure 5, column 4 lines 27-30).

However Citta et al. does not explicitly specify a threshold value for select correlation values.

Krasner teaches a correlator system and method having a threshold value for select correlation values (326 FIG.3A, column 6 lines 55-67, column 10 lines 54-62 wherein the correlation peak is detect via threshold with an algorithm provided '291). Through Kransner's teaching, the correlator system and method is prepared for acquiring and tracking the received signal for synchronizing the received signal.

Therfore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the parallel correlators taught by Krasner implemented in Citta et al.'s Detector 60 for the purpose of providing effective and efficient implementation of correlator to speed up the acquisition process (column 2 lines 1-15 '291)

Regarding **claims 2 & 16**, the combined/modified demodulator and its methods teach the determining device comprises an algorithm that determines if a fractional sample delay would improve the demodulation synchronization timing (326 FIG.3A, column 6 lines 55-67, column 10 lines 54-62 wherein the correlation peak is detect via threshold with an algorithm provided '291).

Regarding **claims 10 & 24**, Citta et al. discloses the interpolation filter (column 12 lines 4-6).

Regarding **claim 29**, Citta et al. discloses a digital circuit provided for implementing the method (Figure 5, Figure 7-Figure 14).

Regarding **claims 41 & 42**, Citta et al. discloses a demodulator and its method for demodulating digital data (Figure 5) comprising: *receiving means* for receiving a digital data signal (42-44 Figure 5 is the receiver) of receiving a digital data signal (42 Figure 5); *correlating means* (158 Figure 10) to correlate the digital signal received from the receiver with a reference training sequence (column 2 lines 21-31, column 3 lines 29-31 wherein the pilot up and down chirps contained in the received signal is a reference training sequence) to produce a correlation value; *verification means* (166 Figure 10) to select correlation values (Figure 8 is an example of correlation results/values); *determining means* to determine if an amount of a fractional sample delay added to a demodulator's symbol sampling timing based on the selected correlation values , in Figure 7 the synchronizer 46 with the feedback from the FPLL 62 (frequency/phase lock loop as *determine device*, column 6 lines 40-44) to determine the improvement (locked or not) and from the Timing block 64 to calculate the timing error (Figure 9-12) for Delay block 68. The delay imposed by the timing block 64 has an integer part and a fraction part (shown in Figure 14,

column 11 lines 60-61), wherein the integer part is for a multiplexer (column 11 lines 64-67) the fractional part is used to determine a fractional of a sample to be advanced or retarded (column 11 line 67-column 12 line 4, Figure 7 66-68-62/64 & column 11 line 60-column 12 line 10 wherein the determination is based on the selected correlation values form the Detector that the timing error provides to the 64 Timing and 68 Delay); *implementing means* (Figure 14 Fraction) implementing the fractional sample delay if said determining device determines that a fractional sample delay would improve the demodulation synchronization timing; and demodulating means for demodulating the digital data signal (50 Figure 5, column 4 lines 27-30).

However Citta et al. does not explicitly specify a threshold value for select correlation values.

Krasner teaches a correlator system and method having a threshold value for select correlation values (326 FIG.3A, column 6 lines 55-67, column 10 lines 54-62 wherein the correlation peak is detect via threshold with an algorithm provided '291). Through Kransner's teaching, the correlator system and method is prepared to acquiring and tracking the received signal for synchronizing the received signal.

Therfore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the parallel correlators taught by Krasner implemented in Citta et al.'s Detector 60 for the purpose of providing effective and efficient implementation of correlator to speed up the acquisition process (column 2 lines 1-15 '291).

Regarding **claim 43**, Citta et al. teaches the reference chirps/samples at the beginning of transmission in Figure 8 the result of the correlation with the reference samples and equation (1) column 5 lines 30-40.

6. Claims 3-7 and 17-21are rejected under 35 U.S.C. 103(a) as being unpatentable over Citta et al. (US 6304619 B1) in view of Krasner (US 6208291 B1) as applied to the claims 1, 10, 15, and 24 above, further in view of Beauvais et al. (US 4025775).

Regarding **claims 3 & 17**, Citta et al. does not explicitly specify using a correlation curve. However, Beauvais et al. teaches exploiting the geometry of a correlation curve to determine a fractional sample delay to improve the demodulation synchronization timing (70, 80 FIG.3, column 6 lines 16-25, FIG.5, FIG.8, column 8 lines 10-50).

Through Beauvais et al.'s teaching, the correlator is capable of performing a correlation with an improved degree sensitivity using the correlation curve technique (column 1 lines 42-45) for synchronizing input signals (Abstract).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Beauvais et al.'s teaching in Citta et al.'s correlation position detector for the purpose of achieving high accurate and sensitive corrrelator (column 1 lines 40-55 '775).

Regarding **claims 4 & 18**, Citta et al. does not explicitly teach comparing the first and last correlation values of the correlation curve that exceed a threshold value. However, Beauvais et al. teaches comparing the first and last correlation values of the correlation curve that exceed a threshold value (60, 70 FIG.3, FIG.7).

Through Beauvais et al.'s teaching, the correlator is capable of performing a correlation with an improved degree sensitivity using the correlation curve technique (column 1 lines 42-45) for synchronizing input signals (Abstract).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Beauvais et al.'s teaching in Citta et al.'s correlation position detector for the purpose of achieving high accurate and sensitive corrrelator (column 1 lines 40-55 '775).

Regarding **claims 5 & 19**, Citta et al. does not explicitly teach counting correlation values that exceed a threshold value. However, Beauvais et al. teaches counting correlation values that exceed a threshold value (65-71-73 FIG.3, 715 FIG.7, column 8 lines 20-50, column 10 lines 1-5, where the correlation values stored).

Through Beauvais et al.'s teaching, the correlator is capable of performing a correlation with an improved degree sensitivity using the correlation curve technique (column 1 lines 42-45) for synchronizing input signals (Abstract).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Beauvais et al.'s teaching in Citta et al.'s correlation position detector for the purpose of achieving high accurate and sensitive corrrelator (column 1 lines 40-55 '775).

Regarding **claims 6-7 & 20-21**, Citta et al. discloses determining an amount of fractional sample delay necessary to improve the demodulation synchronization timing (column 11 lines 20-50, column 11 line 67-column 12 line 10).

7. Claims 8-9, 22-23, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Citta et al. (US 6304619 B1) in view of Krasner (US 6208291 B1) as applied to the claims 1 and 15 above, further in view of Knutson et al. (US 5943369).

Regarding **claims 8 & 22**, Citta et al. does not teach the delay range. However, further Knutson et al. teaches the fractional sample delay is in the range of -0.5 to 0.5 (NUMBERICALLY CONROLLED DELAY FIG.2, column 2 lines 30-40, column 4 lines 50-60).

Through Knutsonet et al.'s teaching, the receiver having variable symbol rate timing recovery is prepared to properly timing the received samples.

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Knutsonet et al.'s NUMBERICALLY CONROLLED DELAY in Citta et al.'s Sync unit (46 Figure 5/Figure 7) for the purpose to have an efficient synchronous design with the chosen range (column 4 lines 55-62 '369).

Regarding **claims 9 & 23**, Citta et al. does not specify the delay range. However, Knutson et al. teaches the fractional sample delay is in the range of -0.5 to 0.5 (NUMBERICALLY CONROLLED DELAY FIG.2, column 2 lines 30-40, column 4 lines 50-60) which includes the group consisting of $\pm 1/4$ and $\pm 1/2$. Refer to the rationale of claims 8 and 22.

Regarding **claim 30**, except explicitly specify a processor, Citta et al. discloses all subject matter claimed (refer to the rejection of claim 1).

However Knutson et al. teaches a digital signal processing system to implementing the method (column 1 lines 5-10). Through Knutson et al.'s teaching, the receiver having a process is prepared to properly timing the received digital samples.

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the DSP taught by Knutson to implement the Citta et al.'s method for the purpose of processing digital data to provide a timing recovery in the digital implementation (column 1 lines 1-25; FIG.1 & column 4 lines 40-46 '369).

8. Claims 14, 28 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Citta et al. (US 6304619 B1) in view of Krasner (US 6208291 B1) as applied to claims 1 and 15 above, and further in view of Nishida et al. (US 6064939).

Regarding **claims 14, 28 & 44**, Citta et al. does not teach the VDL Mode 2 receiver. However, Nishida et al. teaches the VDL receiver in the ATN aircraft data detection device (FIG.4, column 5 line 50-column 6 line5) in the aircraft transceiver.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the demodulator of Citta et al. comprising the demodulator portion of a VDL Mode 2 receiver taught by Nishida et al for the purpose to handle/synchronize the burst of the aircraft system signal and get accurate aircraft signals to have a save surveillance system (column 2 lines 24-30).

9. Claims 31-32, 38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Citta et al. (US 6304619 B1) in view of Knutson et al. (US 5943369) and Broekhoven et al. (US 4894842).

Regarding **claim 31**, Citta et al. discloses a demodulator and its methods for demodulating digital data (Figure 5), comprising: *a receiver* for receiving a digital data signal (42-44 Figure 5 is the receiver); *a correlator* (158 Figure 10) to correlate the digital signal received from the receiver with a reference training sequence (column 2 lines 21-31, column 3 lines 29-31 wherein the pilot up and down chirps contained in the received signal is a reference training sequence) to produce a correlation value; *a verification unit* (166 Figure 10) to select correlation values (Figure 8 is an example of correlation results/values); *a determining device* to

determine if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing (60 Figure 9/Figure 10 & column 9 lines 20-45 wherein Figure 10 is the determining device, Figure 7 66-68-62/64 & column 11 line 60-column 12 line 10 determine improvement of synchronization timing); *an implementing device* (Figure 14 Fraction) implementing the fractional sample delay if said determining device determines that a fractional sample delay would improve the demodulation synchronization timing; and a demodulating device for demodulating the digital data signal (50 Figure 5, column 4 lines 27-30).

However, Citta et al. does not teach I) the computer executable code for implementing and II) a threshold value for select correlation values.

With respect to item I), Krasner teaches a correlator system and method having a threshold value for select correlation values (326 FIG.3A, column 6 lines 55-67, column 10 lines 54-62 wherein the correlation peak is detect via threshold with an algorithm provided '291). Through Kransner's teaching, the correlator system and method is prepared to acquiring and tracking the received signal for synchronizing the received signal.

Therfore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the parallel correlators taught by Krasner implemented in Citta et al.'s Detector 60 for the purpose of providing effective and efficient implementation of correlator to speed up the acquisition process (column 2 lines 1-15 '291)

With respect to item II), further Broekhoven et al. teaches a computer readable medium provided for storing the computer executable code (42 FIG.1, column 4 lines 15-25). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the medium taught by Broekhoven et al. in Citta et al's method for the purpose to store the program

where the DSP equipped to handling, processing and performing the sampling direct sequence receiver efficiently (column 2 lines 5-15). The rejections of other limitations in the claims refer to the rationale of the rejections of claims 2-7, and 30 respectively.

Regarding **claims 32, 38 & 40**, Citta et al. does not specify the computer executable code for implementing. However, Broekhoven et al. teaches a computer readable medium provided for storing the computer executable code (42 FIG.1, column 4 lines 15-25). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the medium taught by Broekhoven et al. in Citta et al's method for the purpose to store the program where the DSP equipped to handling, processing and performing the sampling direct sequence receiver efficiently (column 2 lines 5-15).

The rejections of other limitations in the claims 32 and 38 refer to the rationale of the rejections of claims 2 and 10 respectively.

10. Claims 33-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Citta et al. (US 6304619 B1) in view of Krasner (US 6208291 B1) and Broekhoven et al. (US 4894842) as applied to claim 31 above, and further in view of Beauvais et al. (US 4025775).

Regarding **clam 33-37**, Citta et al. discloses all subject matter claimed (refer to the rejection of claim 1). However, Citta et al. does not except explicitly specify the computer executable code for implementing the method.

Broekhoven et al. teaches a computer readable medium provided for storing the computer executable code (42 FIG.1, column 4 lines 15-25). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the medium taught by Broekhoven et

al. in Citta et al's method for the purpose to store the program where the DSP equipped to handling, processing and performing the sampling direct sequence receiver efficiently (column 2 lines 5-15). The rejections of other limitations in the claims refer to the rationale of the rejections of claims 3-7 and 11 respectively.

Allowable Subject Matter

11. Claims 11-13, 25-27 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest, alone or in a combination, among other things, at least a demodulator and its method as a whole, the combination of elements and features, which includes a multiplier for multiplying first and second samples of each pair of input samples by respective coefficients to obtain two fractional values and an adder or summer for summing the fractional values in a interpolation filter to implement the fractional delay added would improve synchronization timing.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M. Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayanti Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
May 2, 2005

YOUNG T. TSE
PRIMARY EXAMINER